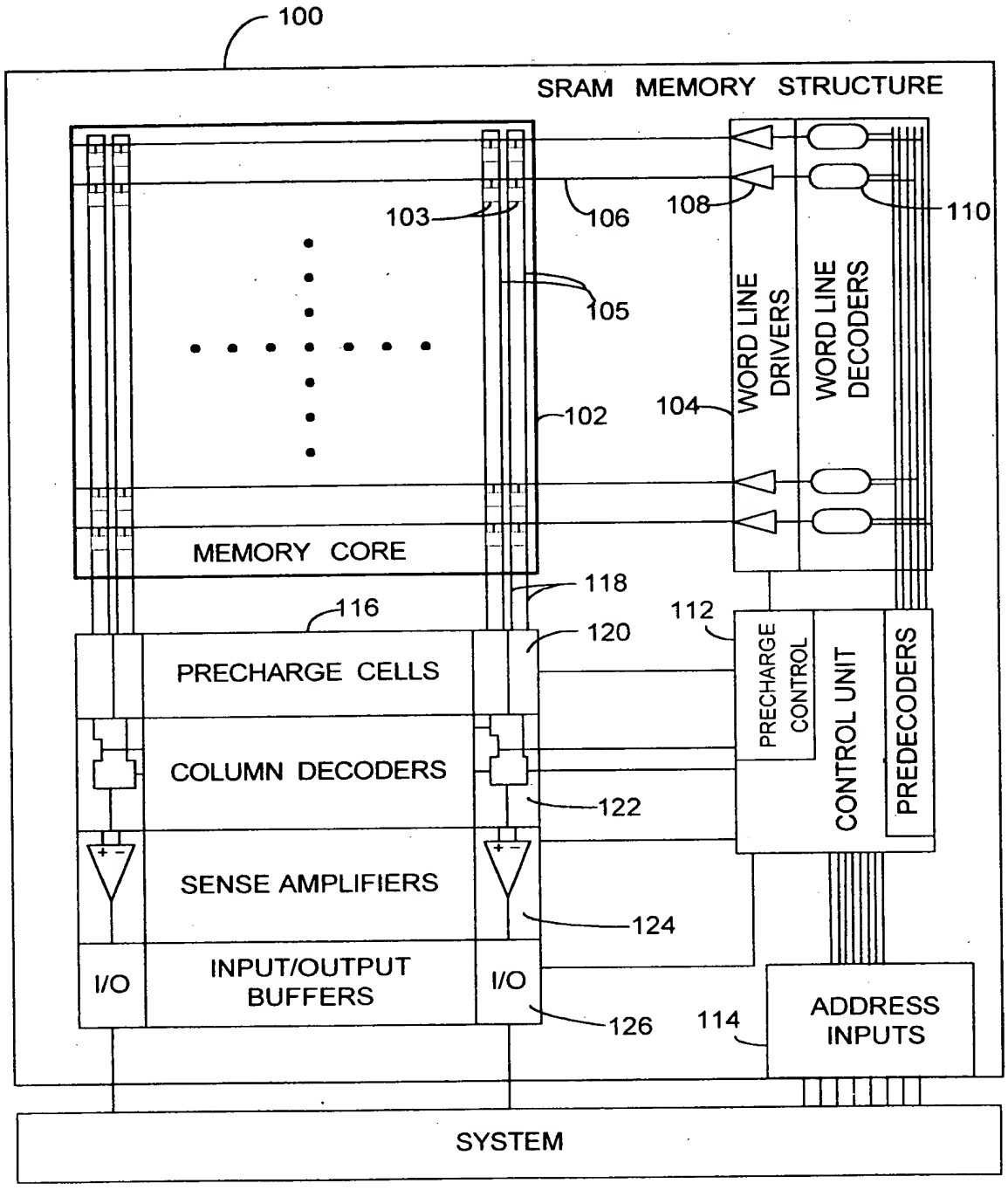
100
SRAM MEMORY STRUCTURE
103
106
108
110
105
WORD LINE DRIVERS
WORD LINE DECODERS
102
104
MEMORY CORE
118
116
120
112
PRECHARGE CELLS
PRECHARGE CONTROL
CONTROL UNIT
PREDECODERS
COLUMN DECODERS
122
SENSE AMPLIFIERS
124
I/O
INPUT/OUTPUT BUFFERS
I/O
126
114
ADDRESS INPUTS
SYSTEM

FIG. 1

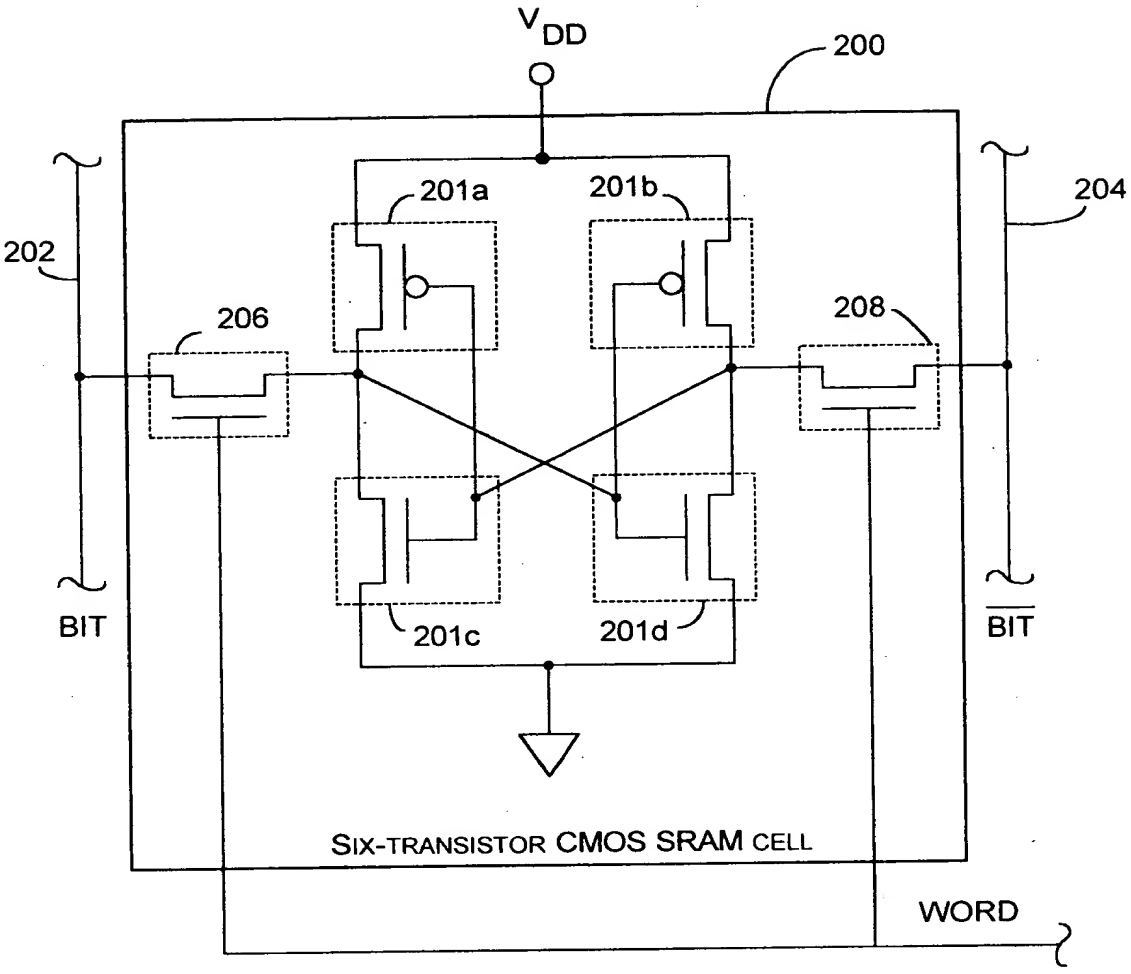
V_{DD}
200
201a
201b
204
202
206
208
BIT
$\overline{BIT}$
201c
201d
SIX-TRANSISTOR CMOS SRAM CELL
WORD

FIG. 2

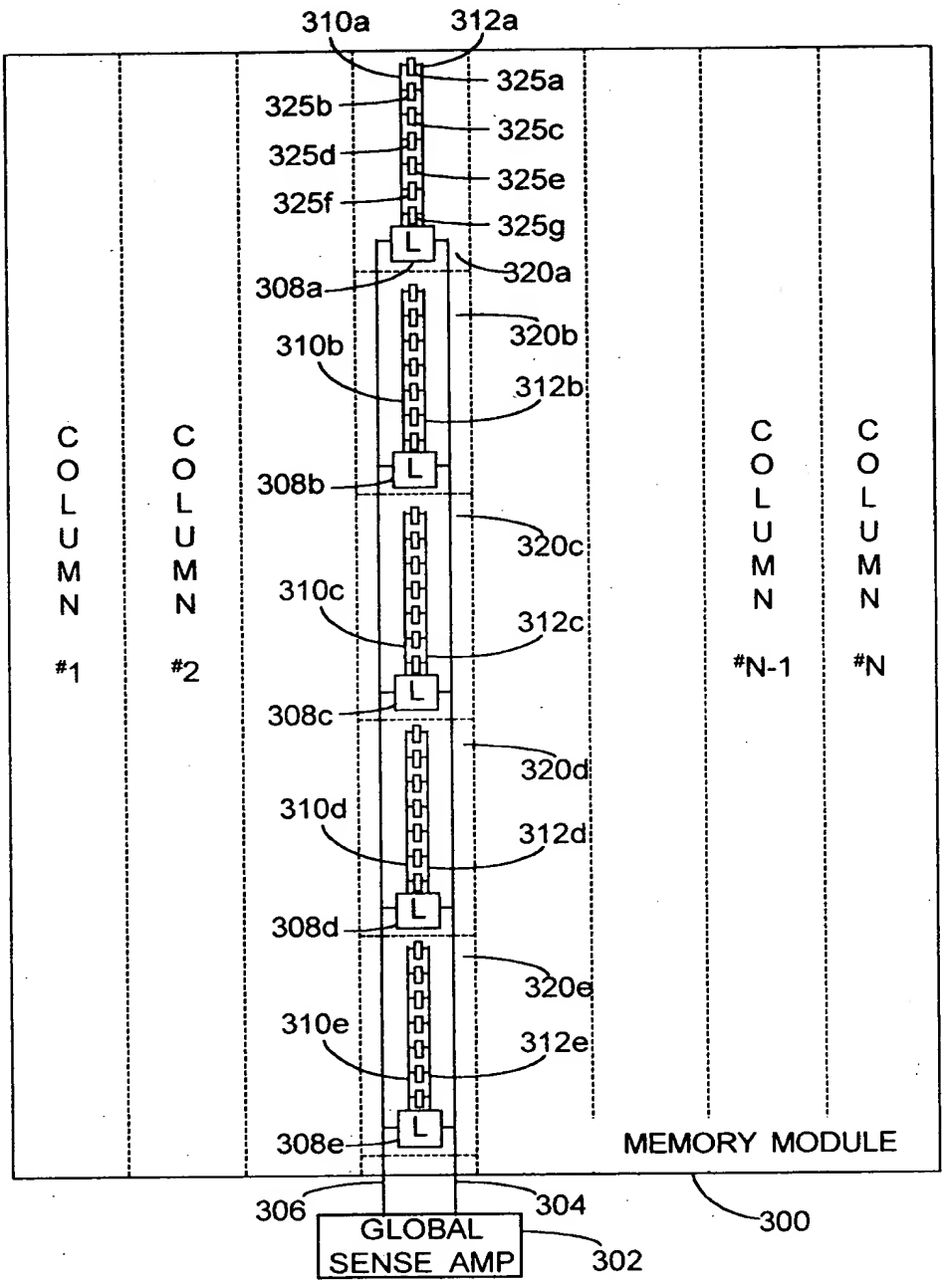
310a
312a
325a
325b
325c
325d
325e
325f
325g
L
320a
308a
320b
310b
312b
308b
320c
310c
312c
308c
320d
310d
312d
308d
320e
310e
312e
308e
COLUMN #1
COLUMN #2
COLUMN #N-1
COLUMN #N
MEMORY MODULE
306
304
GLOBAL SENSE AMP
302
300

FIG. 3

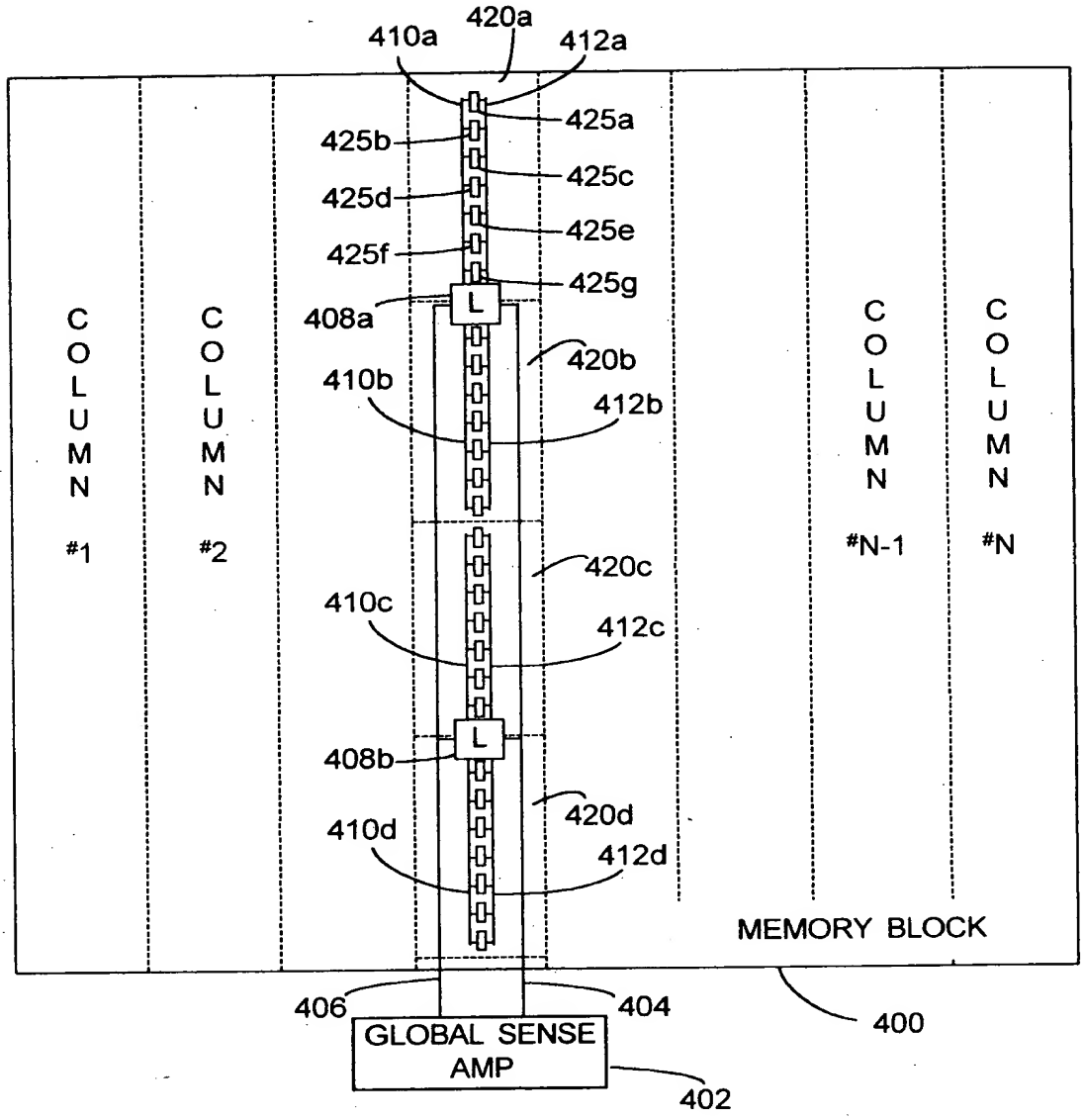
410a
420a
412a
425a
425b
425c
425d
425e
425f
425g
408a
L
420b
410b
412b
COLUMN #1
COLUMN #2
COLUMN #N-1
COLUMN #N
420c
410c
412c
408b
L
420d
410d
412d
MEMORY BLOCK
406
404
400
GLOBAL SENSE AMP
402

FIG. 4

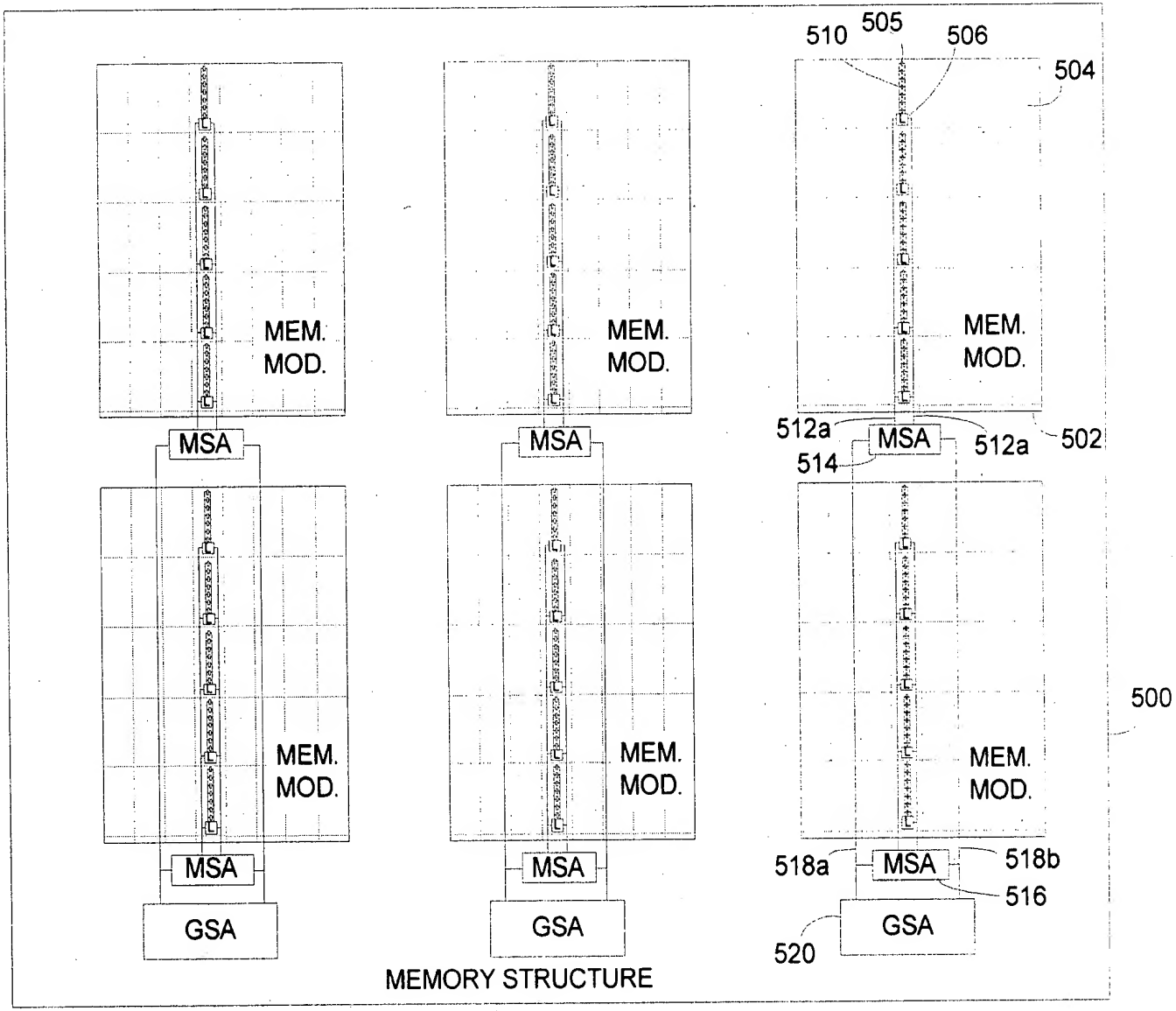
510
505
506
504
MEM.
MOD.
MSA
512a
514
512a
502
500
518a
518b
516
520
GSA
MEMORY STRUCTURE

FIG. 5

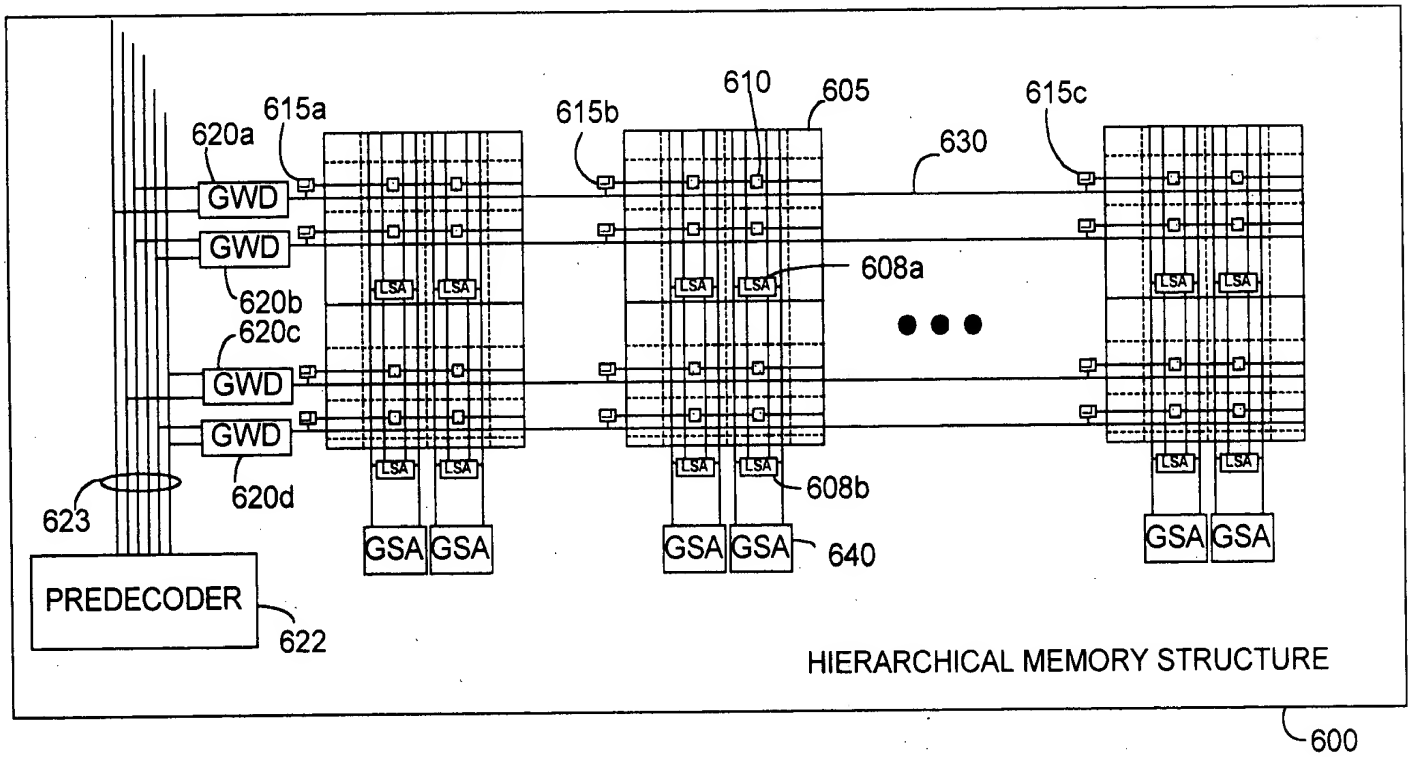
615a
620a
615b
610
605
630
615c
GWD
GWD
620b
620c
GWD
GWD
620d
623
608a
608b
LSA
GSA
640
PREDECODER
622
HIERARCHICAL MEMORY STRUCTURE
600

FIG. 6

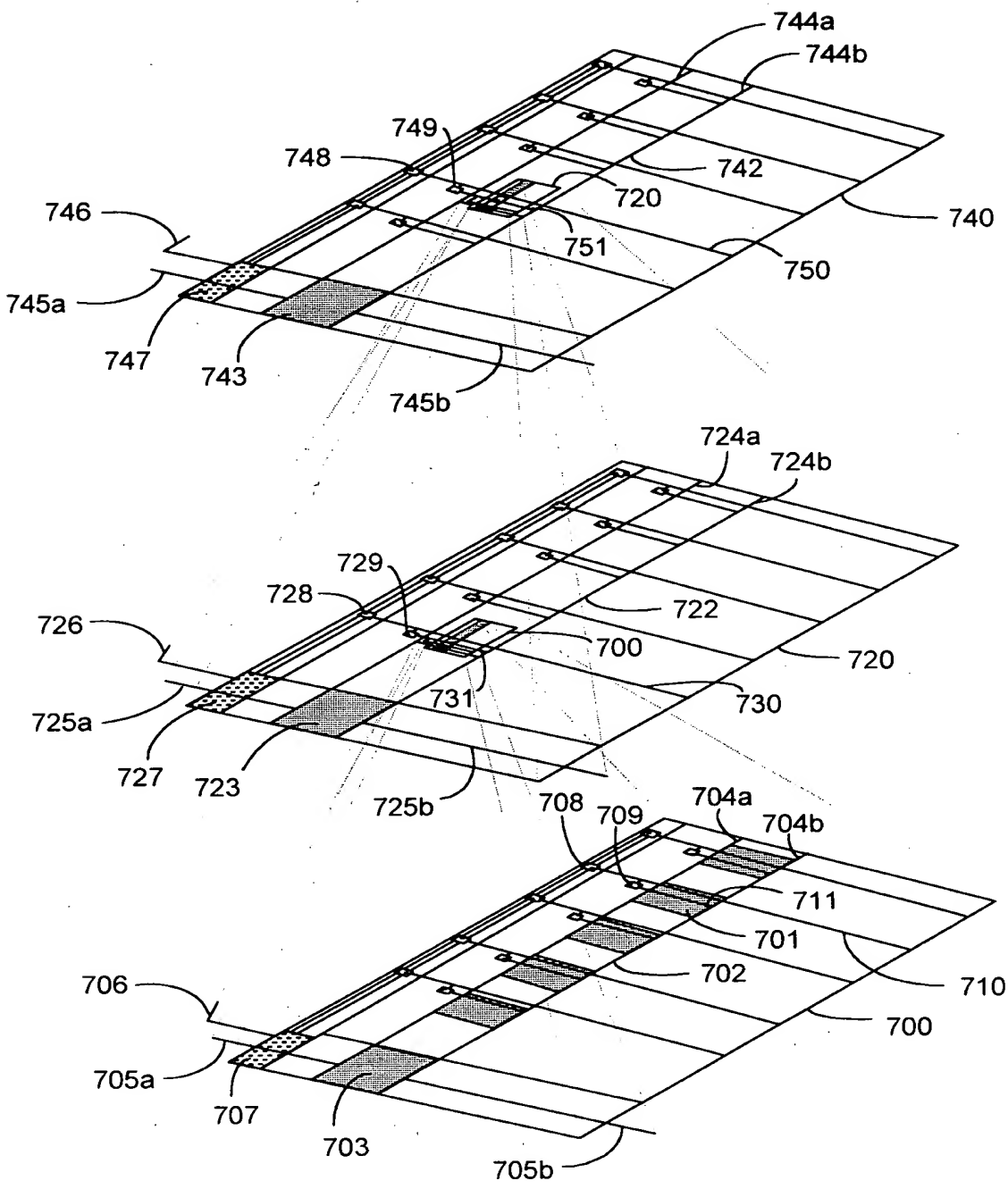
744a
744b
749
748
742
720
746
751
740
750
745a
747
743
745b
724a
724b
729
728
722
726
700
720
731
730
725a
727
723
725b
708
709
704a
704b
711
701
706
702
710
700
705a
707
703
705b

FIG. 7

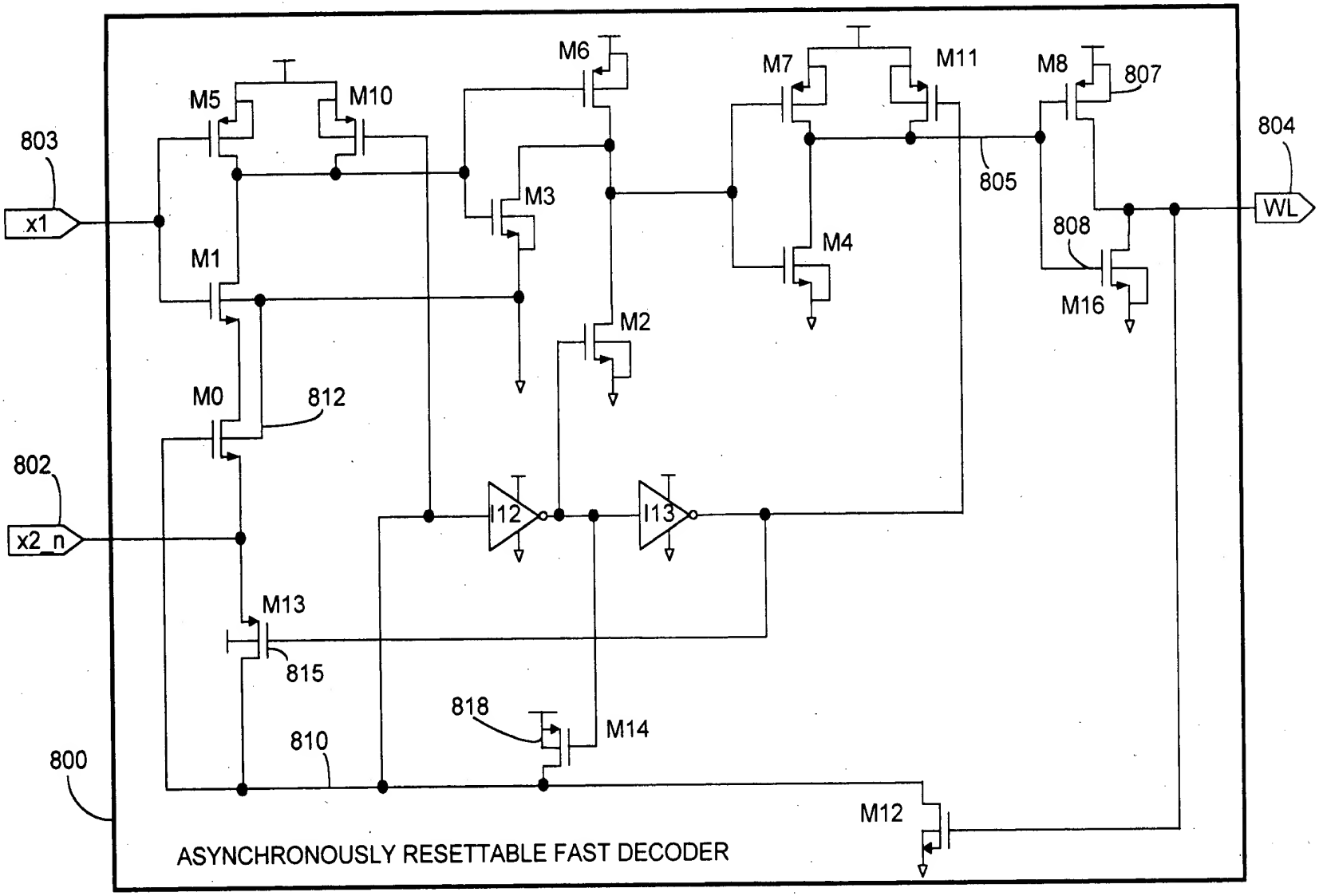
M6
M7
M11
M8
807
M5
M10
803
804
x1
M3
805
WL
M4
M1
808
M16
M2
M0
812
802
I12
I13
x2_n
M13
815
818
M14
810
800
M12
ASYNCHRONOUSLY RESETTABLE FAST DECODER

FIG. 8

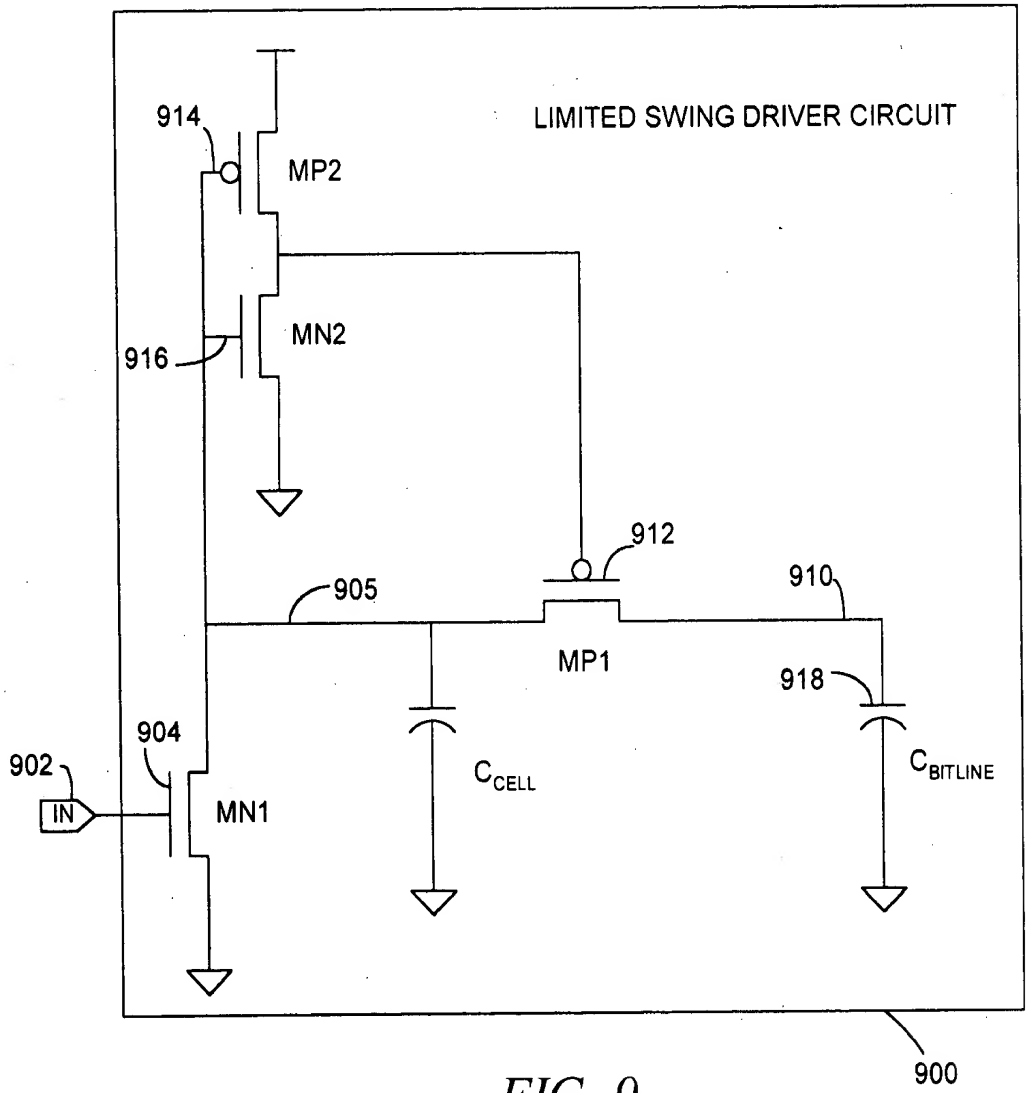
LIMITED SWING DRIVER CIRCUIT
914
MP2
916
MN2
912
905
910
MP1
918
904
902
IN
MN1
C_{CELL}
$C_{BITLINE}$
900

FIG. 9

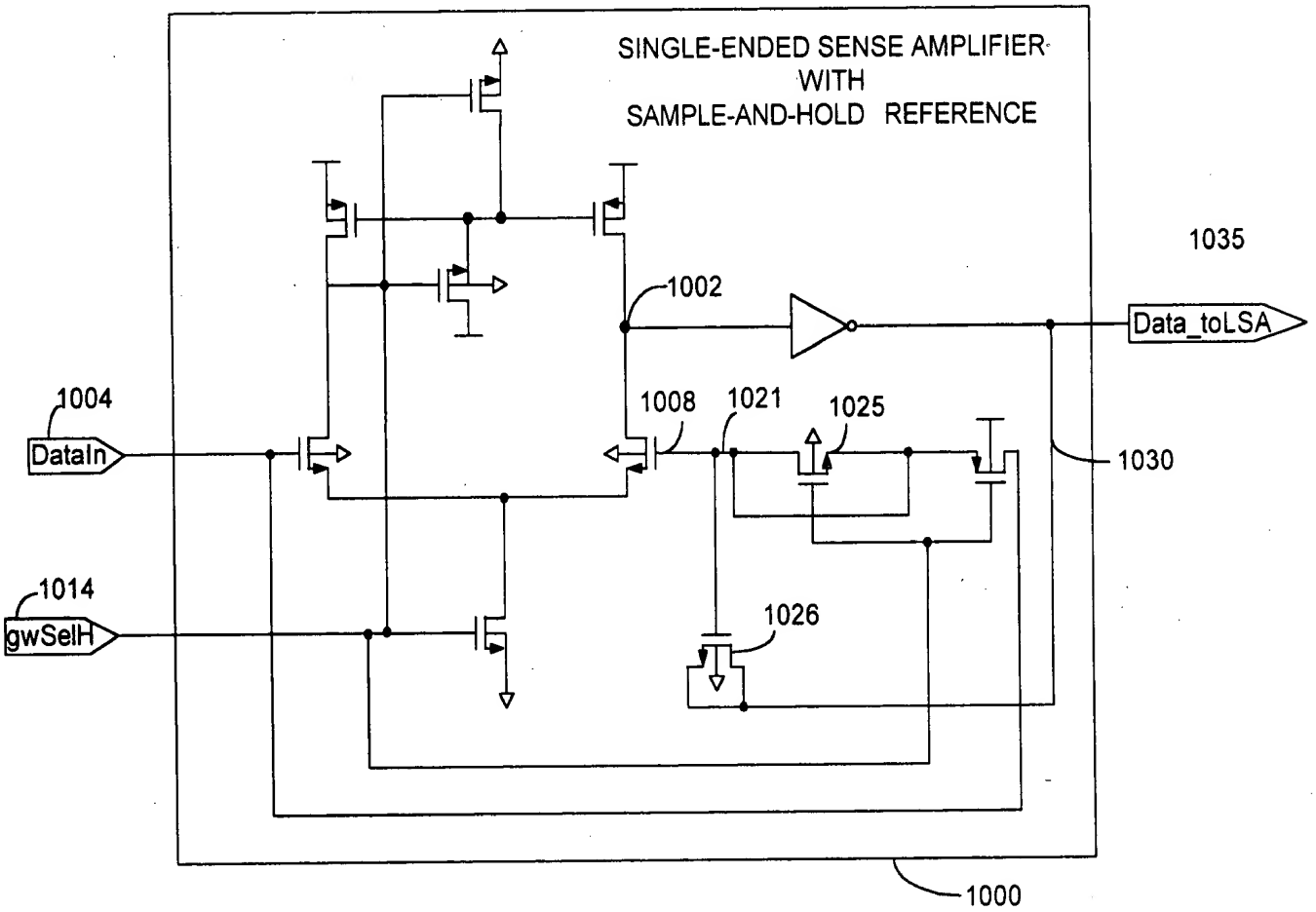
SINGLE-ENDED SENSE AMPLIFIER
WITH
SAMPLE-AND-HOLD REFERENCE
1035
1002
Data_toLSA
1004
DataIn
1008
1021
1025
1030
1014
gwSelH
1026
1000

FIG. 10

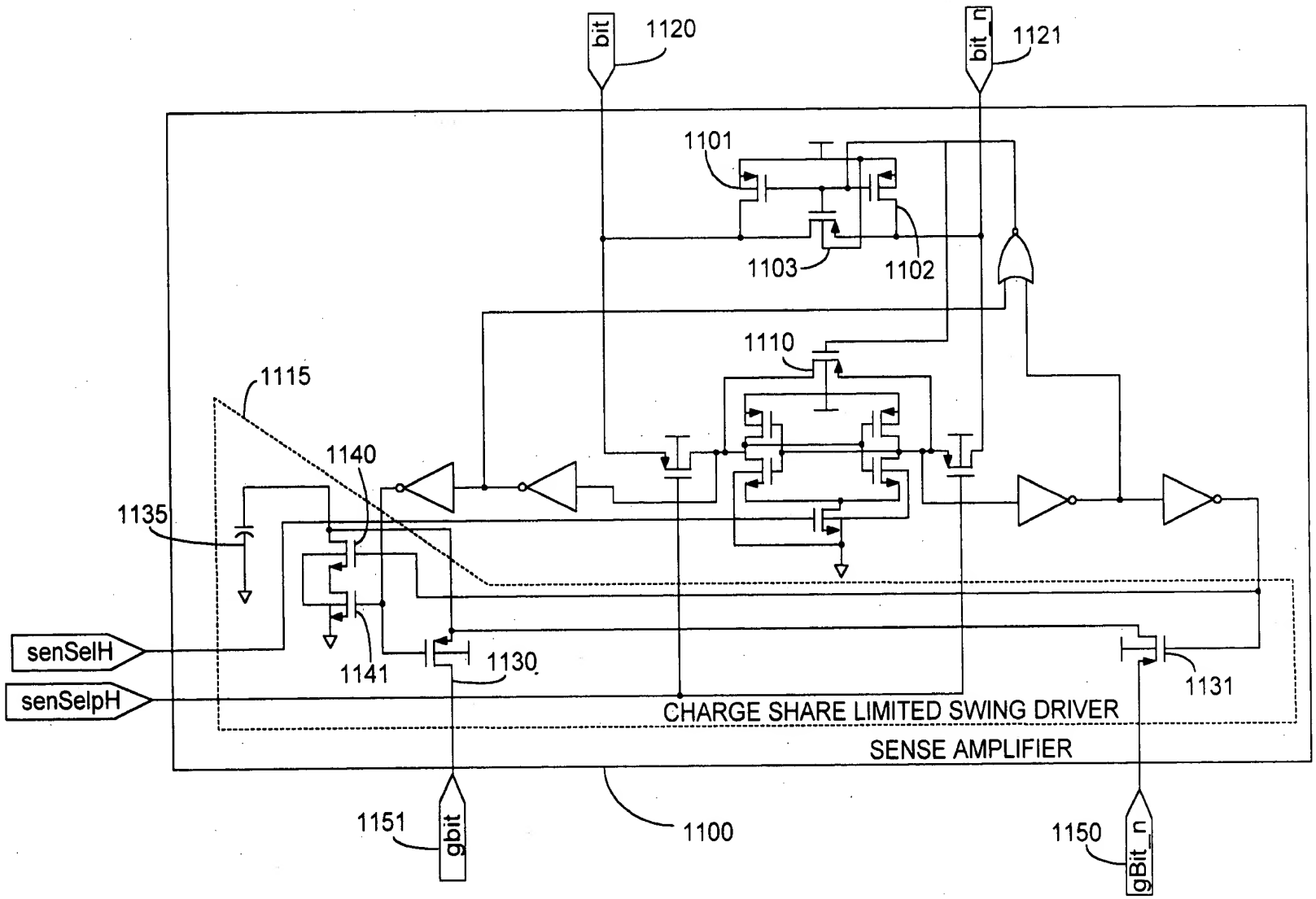

FIG. 11

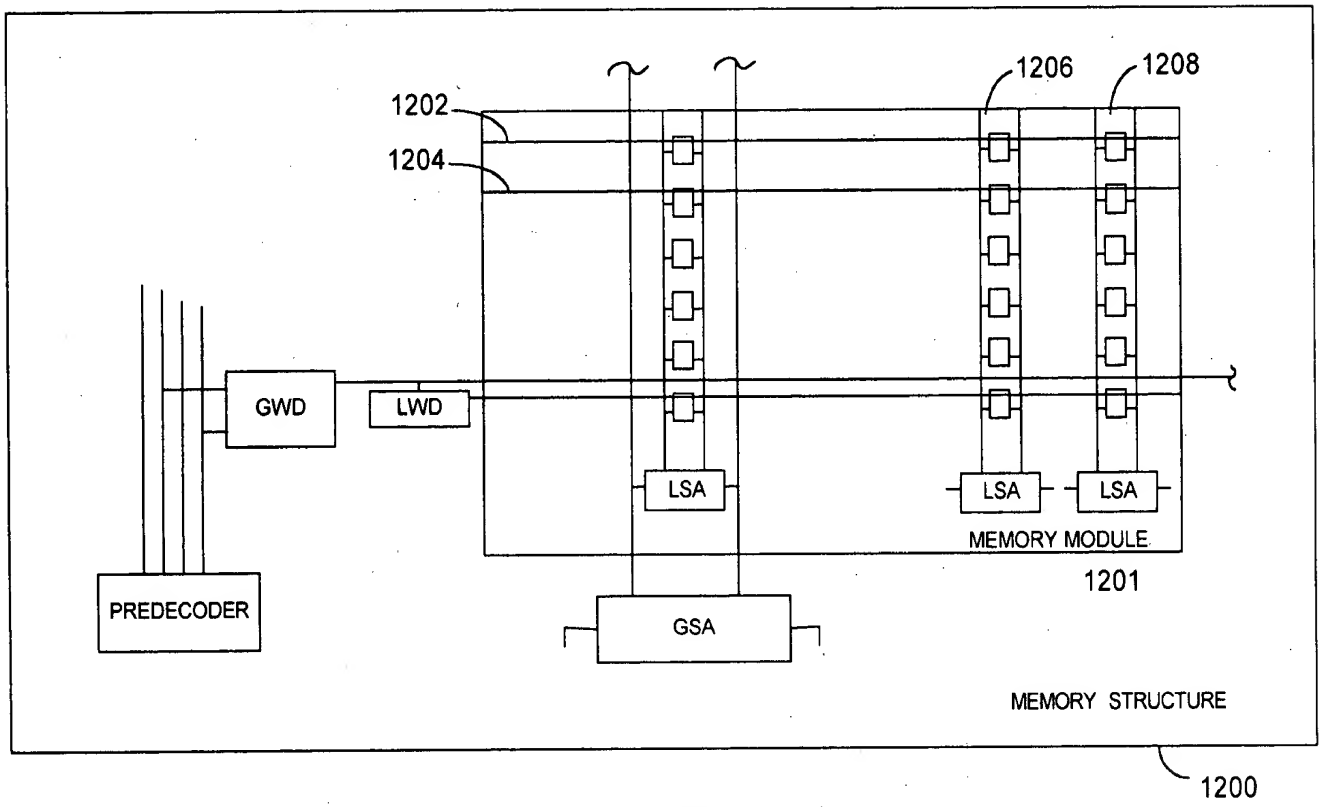
1202
1204
1206
1208
GWD
LWD
LSA
LSA
LSA
MEMORY MODULE
1201
PREDECODER
GSA
MEMORY STRUCTURE
1200

FIG. 12

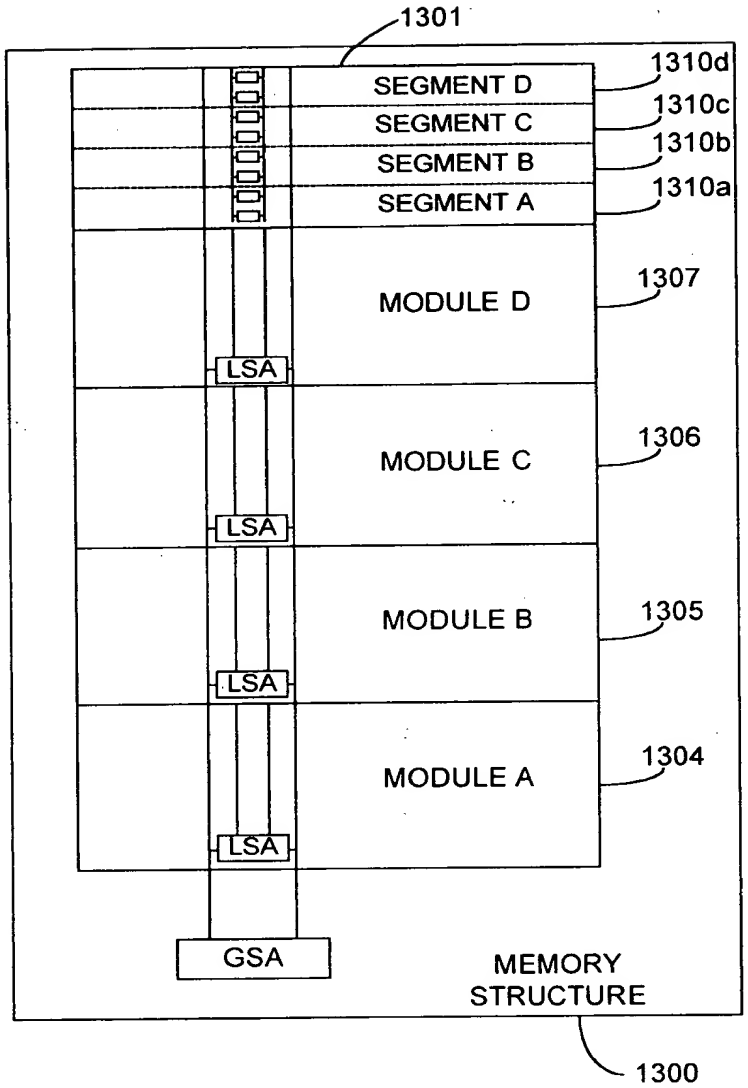
1301
SEGMENT D
SEGMENT C
SEGMENT B
SEGMENT A
1310d
1310c
1310b
1310a
MODULE D
1307
MODULE C
1306
MODULE B
1305
MODULE A
1304
LSA
LSA
LSA
LSA
GSA
MEMORY
STRUCTURE
1300

FIG. 13

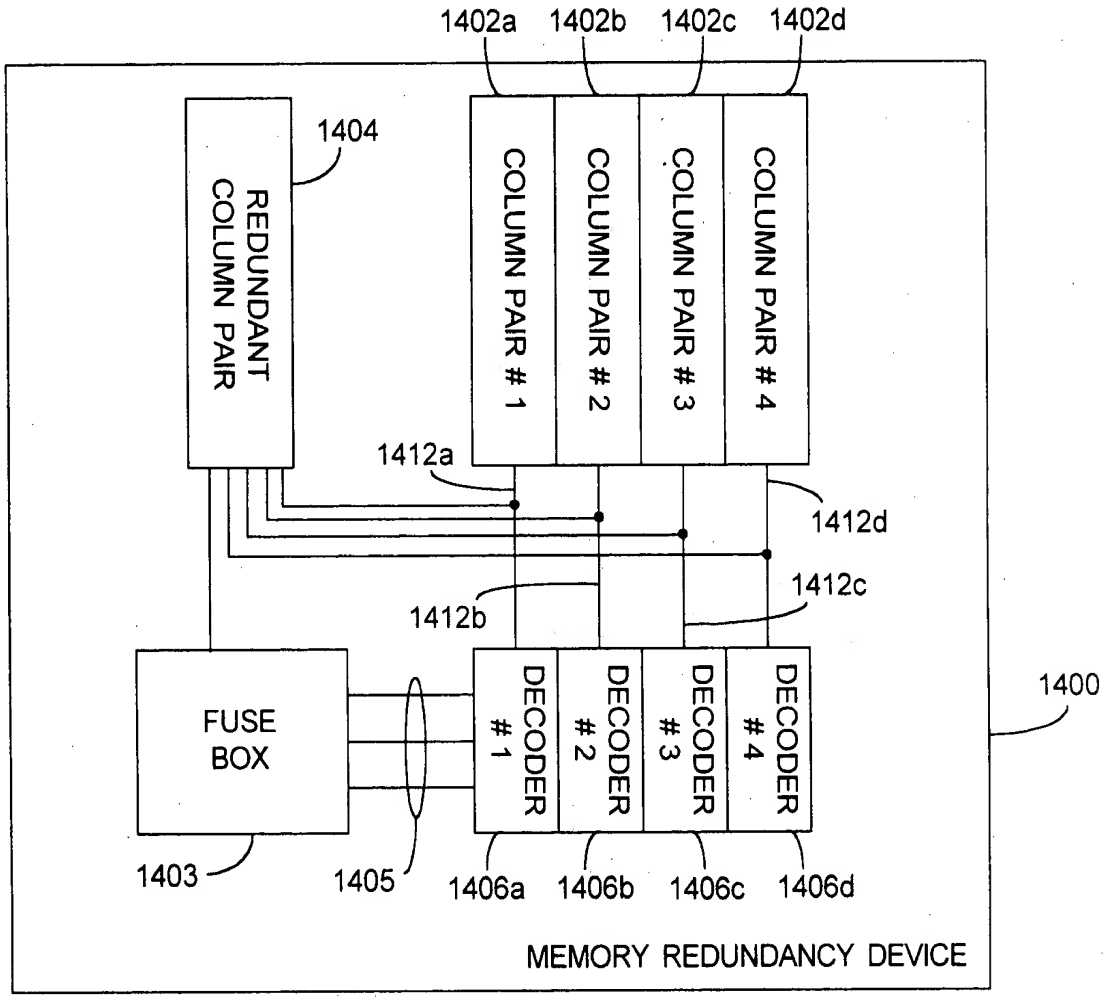
1402a
1402b
1402c
1402d
1404
REDUNDANT COLUMN PAIR
COLUMN PAIR # 1
COLUMN PAIR # 2
COLUMN PAIR # 3
COLUMN PAIR # 4
1412a
1412d
1412c
1412b
FUSE BOX
DECODER # 1
DECODER # 2
DECODER # 3
DECODER # 4
1400
1403
1405
1406a
1406b
1406c
1406d
MEMORY REDUNDANCY DEVICE

FIG. 14

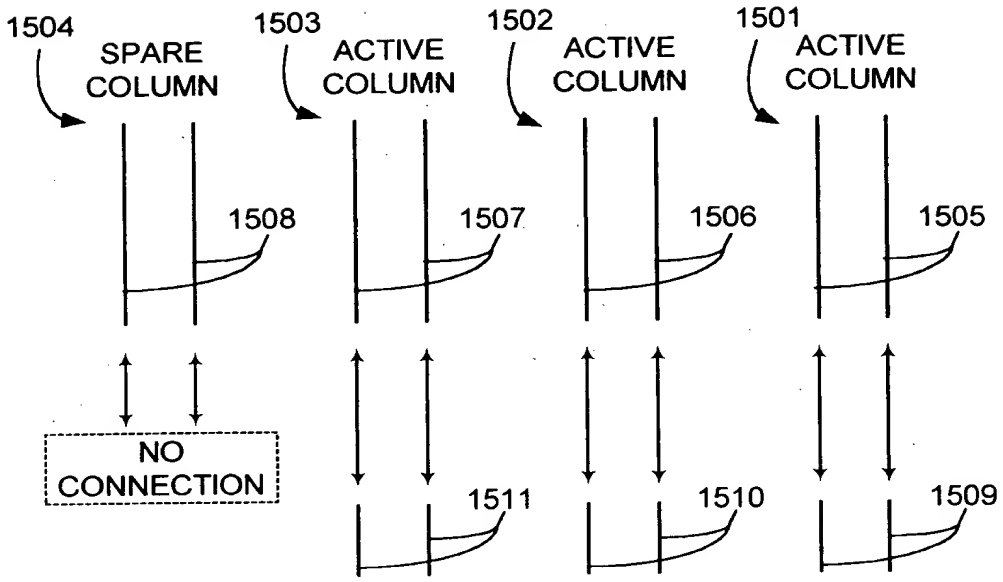

FIG. 15A

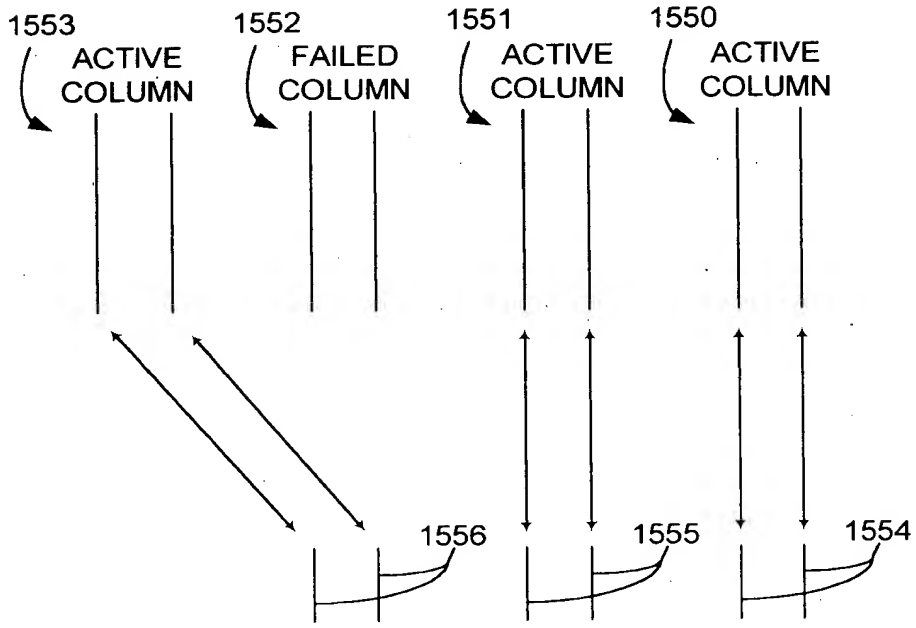

FIG. 15B

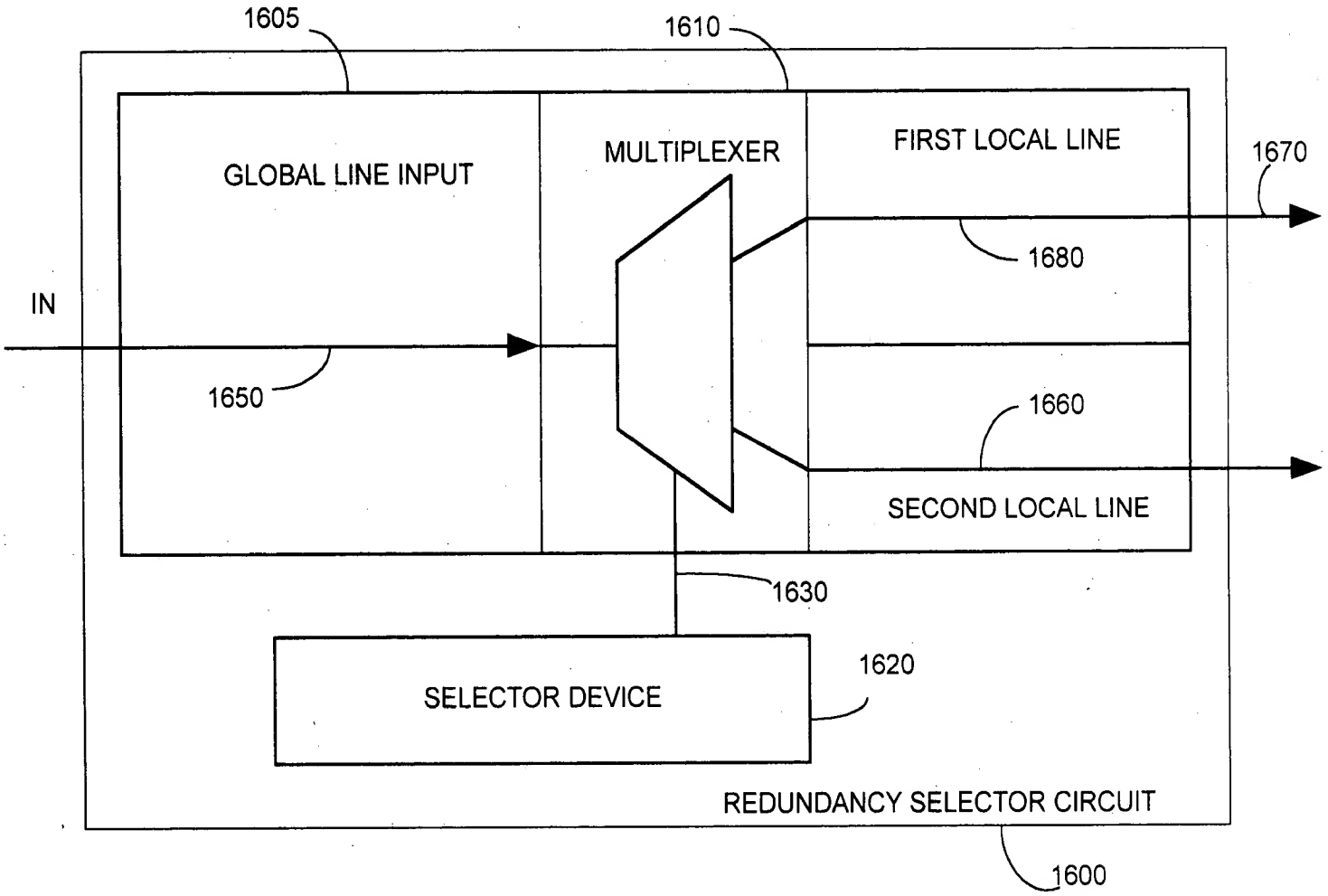
1605
1610
GLOBAL LINE INPUT
MULTIPLEXER
FIRST LOCAL LINE
1670
1680
IN
1650
1660
SECOND LOCAL LINE
1630
1620
SELECTOR DEVICE
REDUNDANCY SELECTOR CIRCUIT
1600

FIG. 16

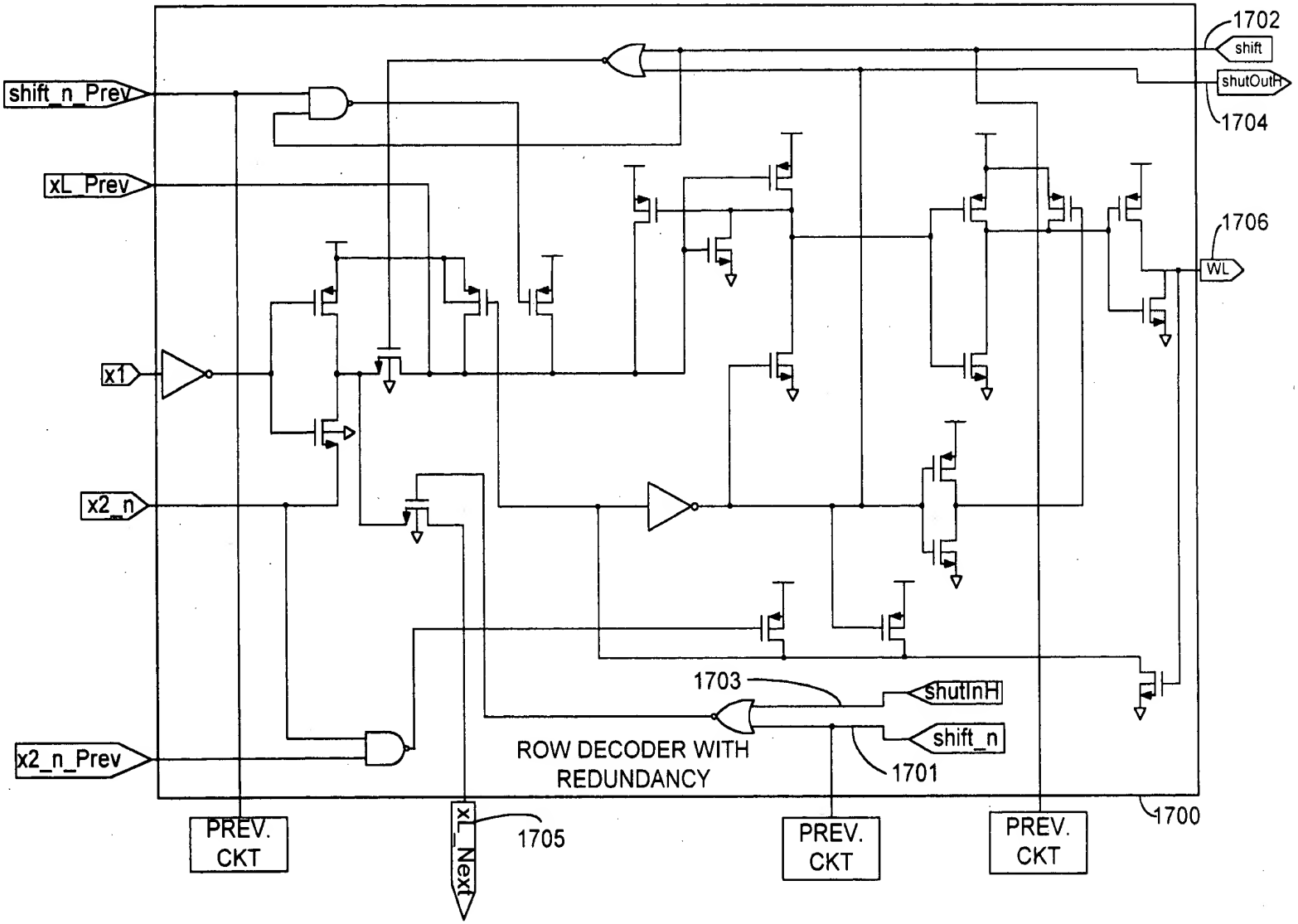
1702
shift
shutOutH
1704
shift_n_Prev
xL_Prev
1706
WL
x1
x2_n
1703
shutInH
shift_n
x2_n_Prev
ROW DECODER WITH
REDUNDANCY
1701
1700
PREV.
CKT
xL_Next
1705
PREV.
CKT
PREV.
CKT

FIG. 17

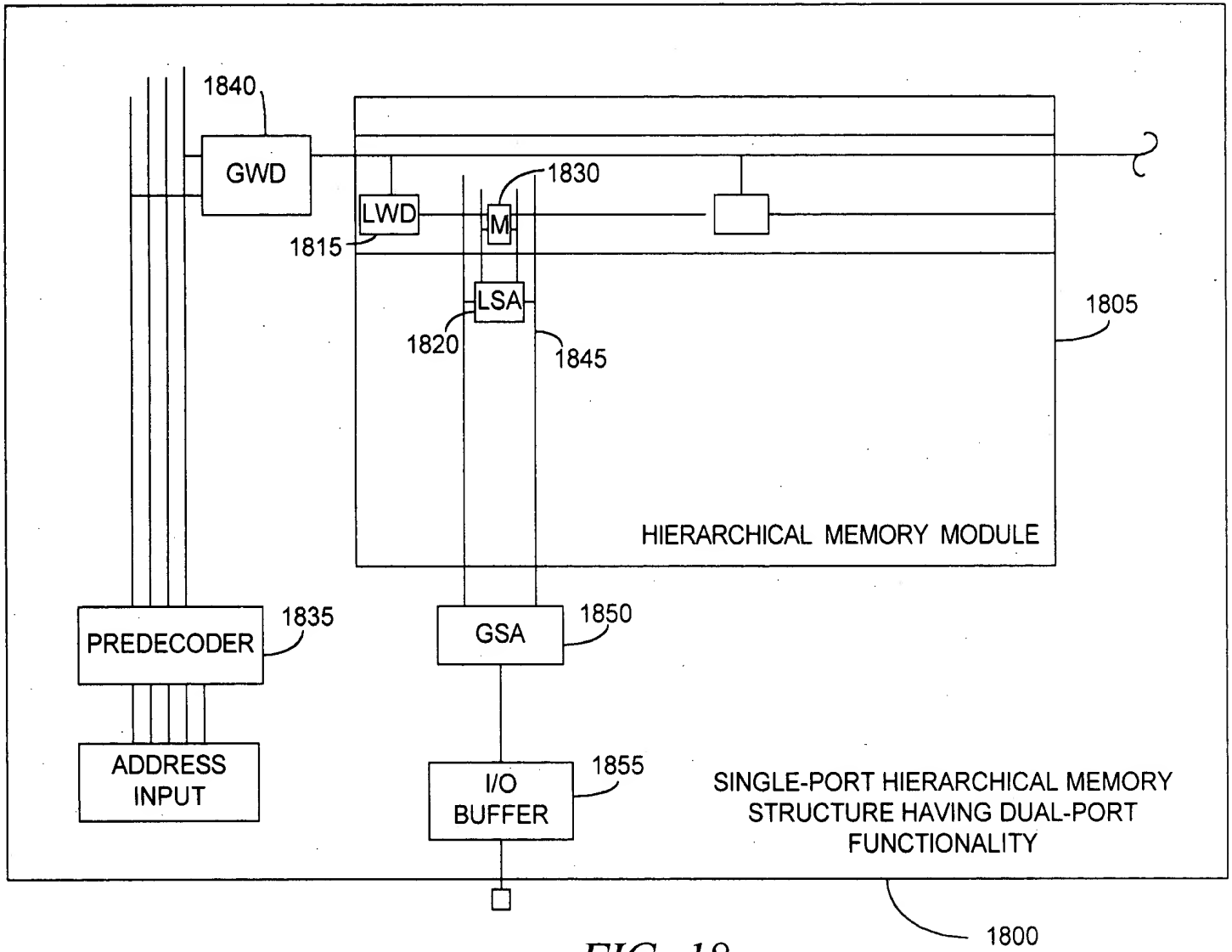
1840
GWD
LWD
1815
1830
M
LSA
1820
1845
1805
HIERARCHICAL MEMORY MODULE
PREDECODER
1835
GSA
1850
ADDRESS INPUT
I/O BUFFER
1855
SINGLE-PORT HIERARCHICAL MEMORY STRUCTURE HAVING DUAL-PORT FUNCTIONALITY
1800

FIG. 18

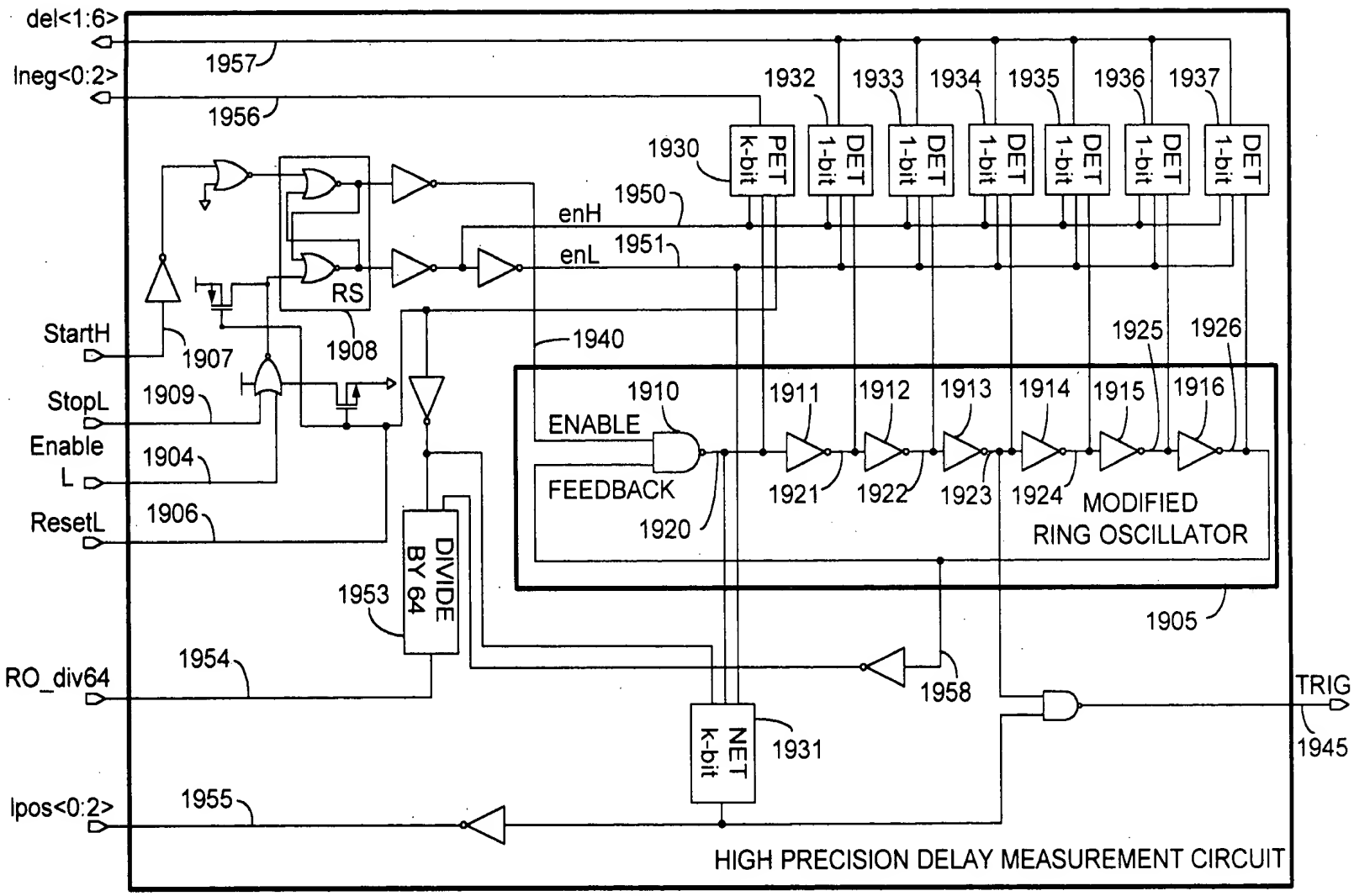
del<1:6>
lneg<0:2>
1957
1956
1932
1933
1934
1935
1936
1937
1930
PET k-bit
DET 1-bit
1950
enH
1951
enL
RS
StartH
1907
1908
1940
1925
1926
StopL
1909
1910
1911
1912
1913
1914
1915
1916
ENABLE
Enable L
1904
FEEDBACK
1921
1922
1923
1924
MODIFIED RING OSCILLATOR
ResetL
1906
1920
DIVIDE BY 64
1953
1905
1954
RO_div64
1958
TRIG
1945
NET k-bit
1931
lpos<0:2>
1955
HIGH PRECISION DELAY MEASUREMENT CIRCUIT

FIG. 19

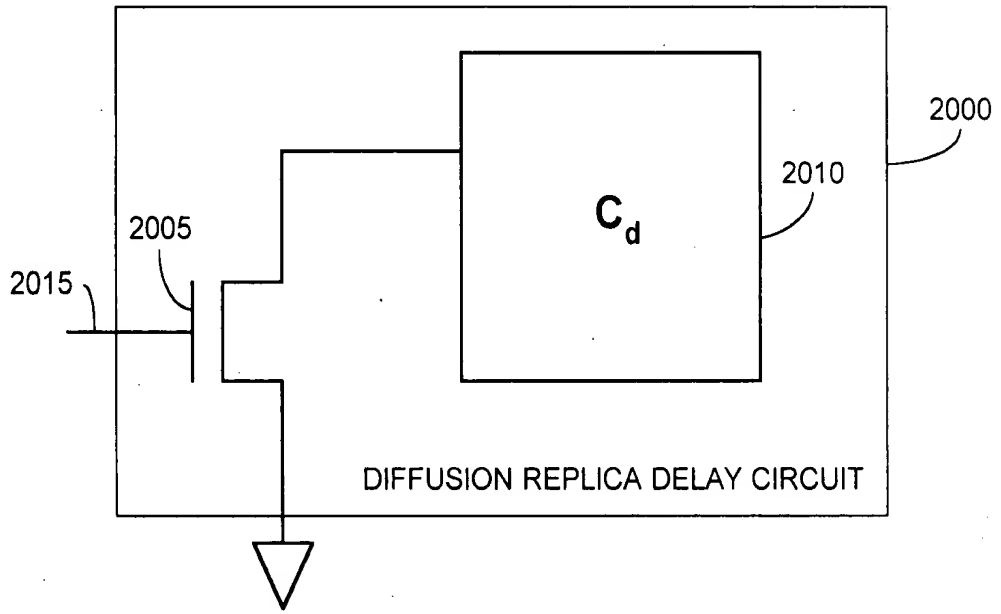

FIG. 20

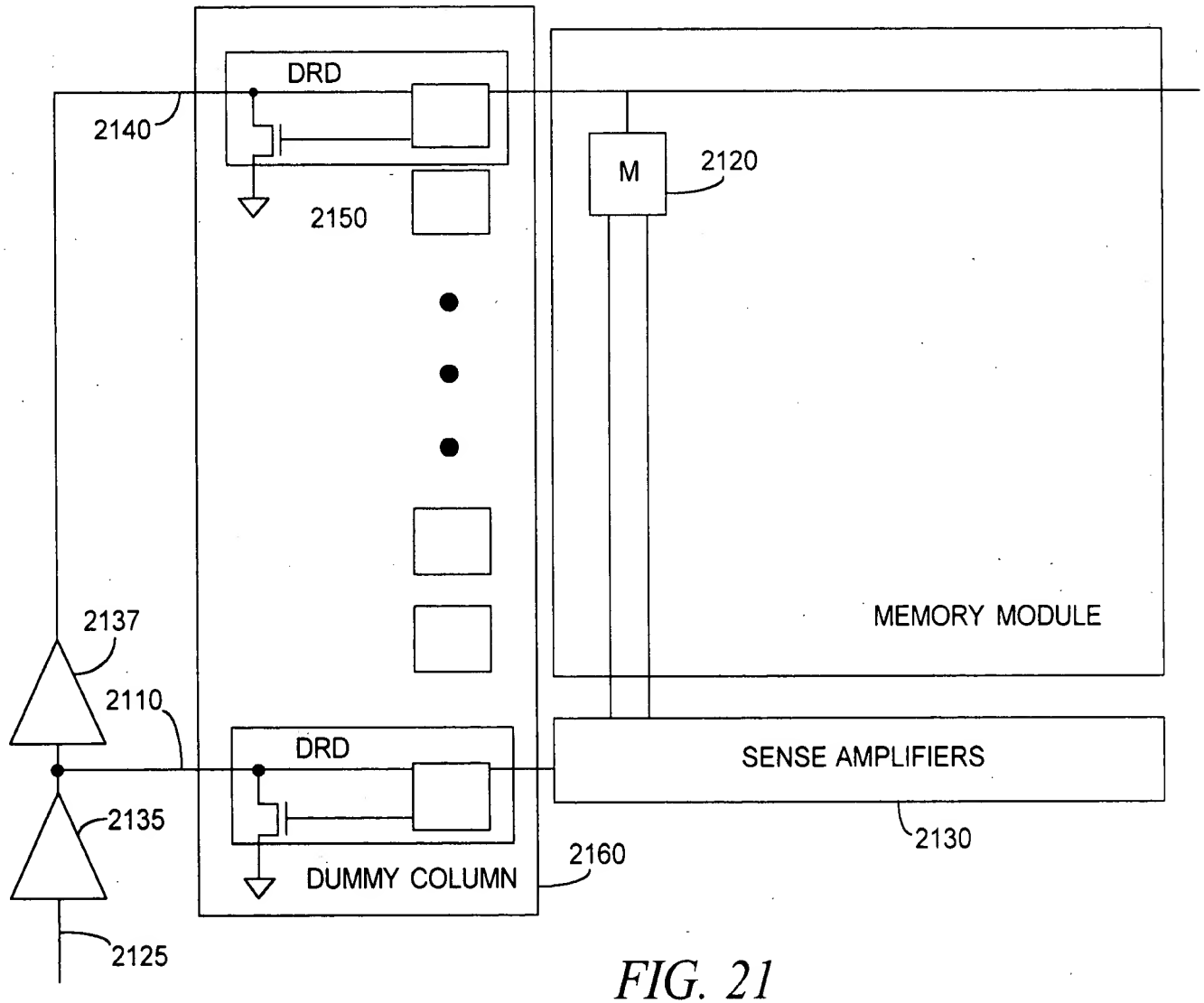
DRD
2140
2150
M
2120
MEMORY MODULE
2137
2110
DRD
SENSE AMPLIFIERS
2135
2130
2160
DUMMY COLUMN
2125

FIG. 21

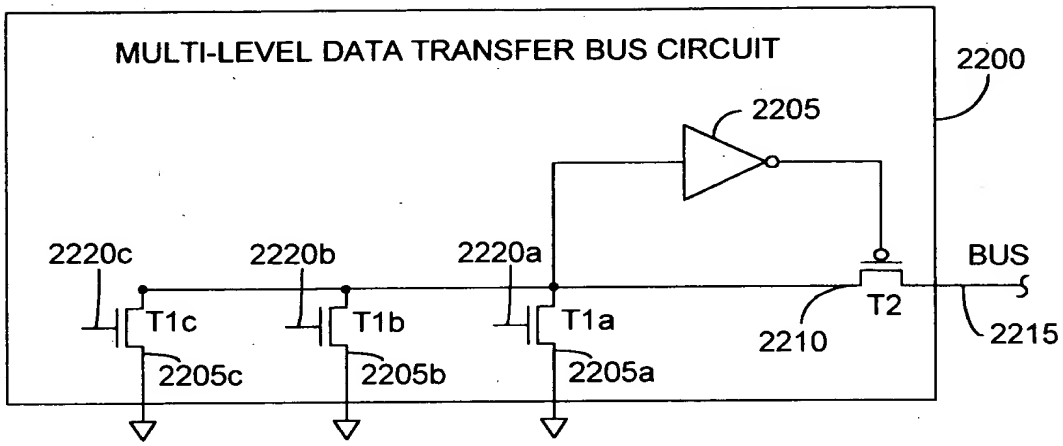

FIG. 22A

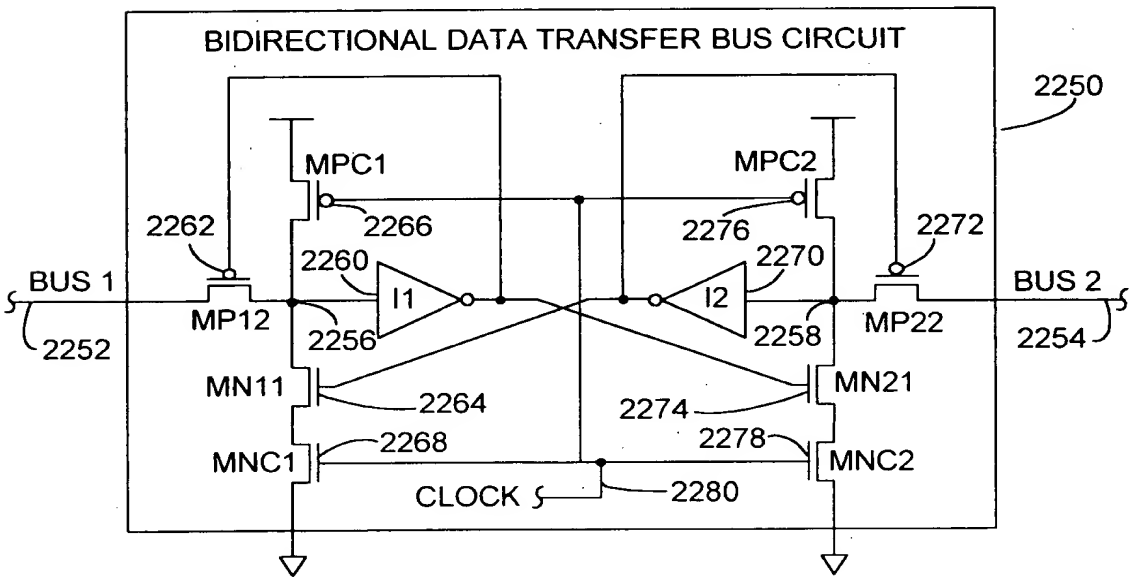

FIG. 22B